REMARKS

Claims 1-5 are pending in the application. Claims 1-2 have been withdrawn from consideration, claim 3 has been amended, and claims 6-10 have been added, leaving claims 3-10 for consideration upon entry of the present Amendment. Applicants respectfully request reconsideration in view of the Amendment.

Applicants have amended the specification as requested by the Examiner.

Claim 3 stands rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's Admitted Prior Art ("AAPA"). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the * * * claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 3, as amended, includes the following limitation: "forming an interlayer insulating film directly on said semiconductor layer, after removal of said mask." The amendment clarifies that the interlayer insulating film is formed directly on the semiconductor layer. See page 10 line 24 to page 11, line 1 of the specification. AAPA does not teach or suggest that limitation, as the ion stopper is located between the interlayer insulating film and the semiconductor layer. In AAPA, the ion stopper results in deterioration of the thin-film transistor characteristics due to impurities contained in the ion stopper remaining inside a finish device. Thus, claim 3 overcomes these problems by having the interlayer insulating film formed directly on the semiconductor layer.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection as to claim 3.

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Tsai et al. (US 5,814,530) ("Tsai"). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

Claims 4 and 5 include all of the limitations of claim 3. Thus, as discussed above, AAPA does not teach or suggest all of the limitations of claims 4 and 5 and Tsai does not remedy the deficiencies. Accordingly, Applicants respectfully request that the Examiner withdraw the rejection as to claims 4 and 5.

Applicants have also added new claims 6-10. As the references do not teach or suggest all of the limitations of those newly added claims, Applicants respectfully request that the Examiner allow those claims.

In addition, attached hereto is a marked-up version of the changes made to the application. The attached page is captioned "**Version with Markings to Show Changes Made.**"

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicants' attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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MARKED UP VERSION TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the paragraph beginning on page 2, line 4 in "marked up" format, as follows:

Step 1: As shown in Fig. 1A, a conductive film of a refractory (high-melting point) metal such as chromium is formed on the glass substrate 51. The conductive film is etched in a predetermined pattern to form a gate electrode 52. Next, a gate insulating film ~~63~~53, which is a laminated structure of a silicon dioxide and a silicon nitride, is formed covering the gate electrodes 52, and then a semiconductor layer 54 of a silicon, and an ion stopper 55 of a silicon dioxide are sequentially formed.

IN THE CLAIMS:

Please amend claim 3 in "marked up" format, as follows:

3. (Marked up/Amended) A method for manufacturing a bottom gate-type thin-film transistor on a transparent insulating substrate, comprising the steps of:

forming a gate electrode on a transparent substrate;

forming a gate insulating film on said gate electrode;

forming a semiconductor layer on said gate insulating film;

forming a mask on said semiconductor layer corresponding to said gate electrode;

doping impurities selectively into said semiconductor layer, using said mask; and

forming an interlayer insulating film directly on said semiconductor layer, after removal of said mask.